(DE3-7) D Flip-Flop

Aim of experiment

This experiment will examine the operation of the D flip-flop gate and compare the expected outputs to the truth tables for this device.

Apparatus

Prototyping Board– DC Power Supply 5V or 9V Battery – Light Emitting Diode (LEDs) – Digital ICs: 7474 D Flip-Flop Gate & 7402 & 7408 & 7400 – Connection wires.

Theory of experiment

All logical circuits we have been working on till now were simple in the sense that the result does not depend on anything else, but the current input. This type of circuits is called "combinational". In contrast, predicting the output of a sequential circuit takes not only present input conditions, but also the past sequence of inputs. This results in the ability of a sequential circuit to "remember" past inputs in order to produce current outputs.

Flip-flops are the most common and basic memory devices used for information storage in sequential circuits. A flip-flop can stay in one of two logical states. To change its state we need a new input signal. This makes the flip-flop a 1 bit memory device. There are three basic types of flip-flops:

• Memory flip-flops have special inputs to be set or reset. The flip-flop preserves its state as long as there is no new input signal

• Delay flip-flops output the state their input had one cycle ago. If the input signal changes at step n the output changes at step n+1

• Toggle flip-flop or "T" flip-flop changes its output on each clock cycle if the input given to T is high (or 1). If the input of T is low (or 0) the output does not change, meaning it is preserved.

(a) *JK* Flip-Flop				(b) *SR* Flip-Flop			
J	K	$Q(t+1)$	Operation	S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change	0	0	$Q(t)$	No change
0	1	0	Reset	0	1	0	Reset
1	0	1	Set	1	0	1	Set
1	1	$\overline{Q}(t)$	Complement	1	1	?	Undefined

(c) *D* Flip-Flop			(d) *T* Flip-Flop		
D	$Q(t+1)$	Operation	T	$Q(t+1)$	Operation
0	0	Reset	0	$Q(t)$	No change
1	1	Set	1	$\overline{Q}(t)$	Complement

Table 1: Truth table for different flip-flop

Delay (D) Flip-Flop

As the name implies the purpose of a D FF is to temporary store (or delay) a single bit. A signal of 0 or 1 present at the input D is transferred to the output Q whenever the clock CLK is set to 1. Figure 1 shows the gate symbol of a D flip-flop.

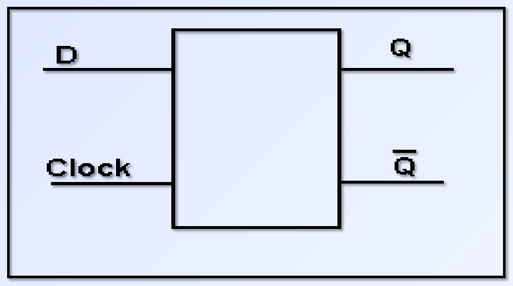


Figure 1. Gate symbol of a D flip-flop

The D flip-flop can be Construction from NAND-latch as shown in Figure 2.

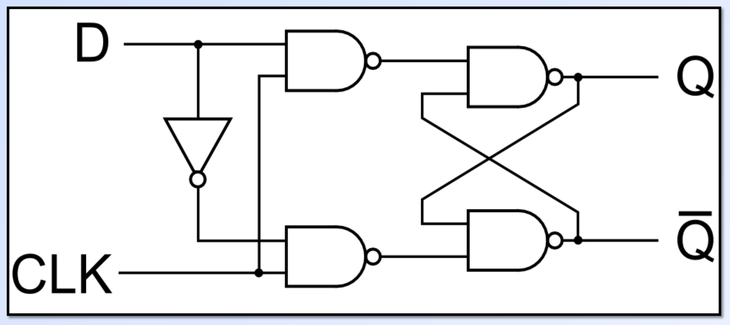


Figure 2. Construction D flip-flop from NAND-latch

The D type flip-flop has one data input 'D' and a clock input. The circuit edge triggers on the clock input. The flip-flop also has two outputs Q and Q' (where Q' is the reverse of Q).

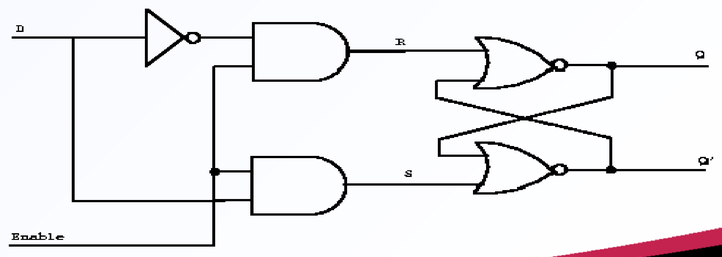
The operation of the D type flip-flop is as follows: Any input appearing (present state) at the input D, will be produced at the output Q in time T+1 (next state). e.g. if in the present state we have D = 0 and Q = 1, the next state will be D = anything and Q = 0. Knowing the above, we can now generate the state change table.

Input	Circuit Action
D	Q (Time t+1)
0	0
1	1

Procedures

First Experiment:

1. Connect the circuit as shown in following figure use 7408 & 7402 logic gates in the Prototyping board.
2. Switch Enable switch on and change switches 1 on and off and push bottom to show the output of LEDS.
3. Record the results in the following table.



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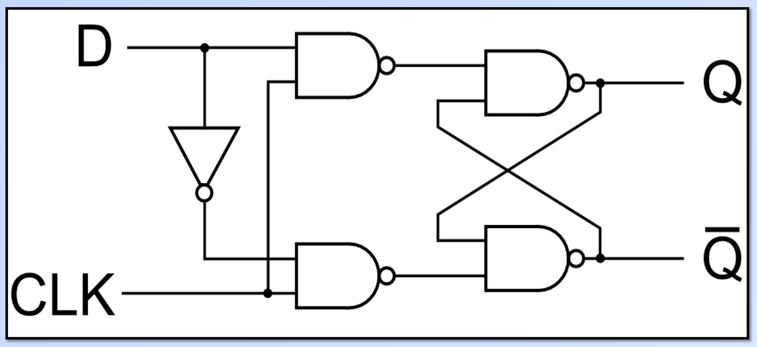
Switch 1 (D)	LED output (Q)
0	
1	
0	
1	

Second Experiment:

1. Connect the circuit as shown in following figure use 7400 logic gates in the Prototyping board.
2. Switch enable switch on and change switches 1 on and off and push bottom to show the output of LEDS.
3. Record the results in the following table.

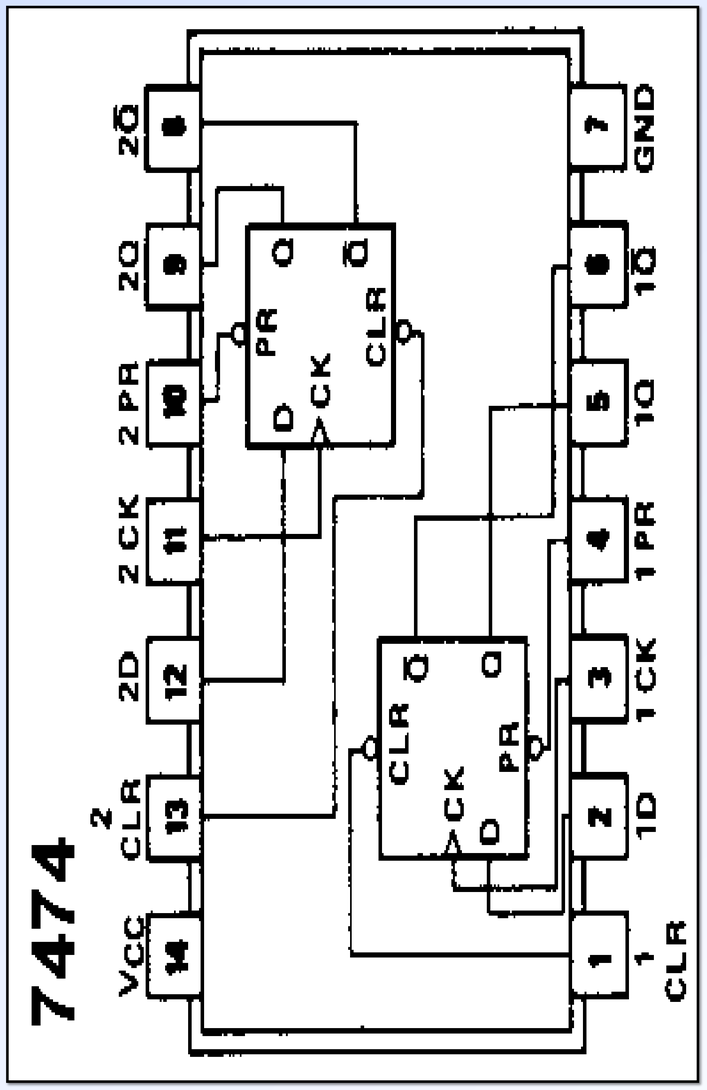


Switch 1 (D)	LED output (Q)
0	
1	
0	
1	

Third Experiment:

4. Put the 7474 D flip-flop Gate shown in the Prototyping board.
5. Connect the pin 14 to 5 V and pin 7 to ground.
6. Connect pin 2 (D) to input switches in Prototyping board, and pin 3 (Clock) to push bottom.
7. Connect pin 5 (Q) to output LED.
8. Change switches 1 on and off and push bottom to show the output of LEDS.
9. Record the results in the following table.

Switch 1 (D)	LED output (Q)
0	
1	
0	
1	



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