

(DE3-6) SR Flip-Flop

Aim of experiment

This experiment will examine the operation of the SR flip-flop gate and compare the expected outputs to the truth tables for this device.

Apparatus

Prototyping Board– DC Power Supply 5V or 9V Battery – Light Emitting Diode (LEDs) – Digital ICs: 7402 NOR Gate & 7400 NAND Gate – Connection Wires.

Theory of experiment

All logical circuits we have been working on till now were simple in the sense that the result does not depend on anything else, but the current input. This type of circuits is called “combinational”. In contrast, predicting the output of a sequential circuit takes not only present input conditions, but also the past sequence of inputs. This results in the ability of a sequential circuit to “remember” past inputs in order to produce current outputs.

Flip-flops are the most common and basic memory devices used for information storage in sequential circuits. A flip-flop can stay in one of two logical states. To change its state we need a new input signal. This makes the flip-flop a 1 bit memory device. There are three basic types of flip-flops:

- Memory flip-flops have special inputs to be set or reset. The flip-flop preserves its state as long as there is no new input signal
- Delay flip-flops output the state their input had one cycle ago. If the input signal changes at step n the output changes at step $n+1$

- Toggle flip-flop or “T” flip-flop changes its output on each clock cycle if the input given to T is high (or 1). If the input of T is low (or 0) the output does not change, meaning it is preserved.

(a) JK Flip-Flop				(b) SR Flip-Flop			
J	K	$Q(t+1)$	Operation	S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change	0	0	$Q(t)$	No change
0	1	0	Reset	0	1	0	Reset
1	0	1	Set	1	0	1	Set
1	1	$\bar{Q}(t)$	Complement	1	1	?	Undefined

(c) D Flip-Flop			(d) T Flip-Flop		
D	$Q(t+1)$	Operation	T	$Q(t+1)$	Operation
0	0	Reset	0	$Q(t)$	No change
1	1	Set	1	$\bar{Q}(t)$	Complement

Table 1: Truth table for different flip-flop

Set Reset (SR) Flip-flop

A simple memory flip-flop is the SR FF. This device has two inputs - S for setting and R for resetting the flip-flop (hence its name). The SR flip-flop preserves its states as long as the inputs S and R are 0. If it receives a set signal, it turns to 1, regardless of its former state. A reset signal enforces a 0 state. This behavior is illustrated by the truth table below (Q^t is the preceding state of Q^{t+1}).

S	R	Q^t	Q^{t+1}	functionality
0	0	0	0	Both inputs are 0, the state is preserved
0	0	1	1	
0	1	0	0	The reset input is 1, the FF is set to 0
0	1	1	0	
1	0	0	1	The set input is 1, the FF is set to 1
1	0	1	1	
1	1	0	X	Both inputs are 1, the FF's behavior cannot be predicted
1	1	1	X	

Table 2: Truth table for SR flip-flop

The most common realizations of SR FFs are based on NOR or NAND gates. *Figure 1* shows a typical NOR-gate core circuit of an SR FF and *figure 2* shows its gate symbol.

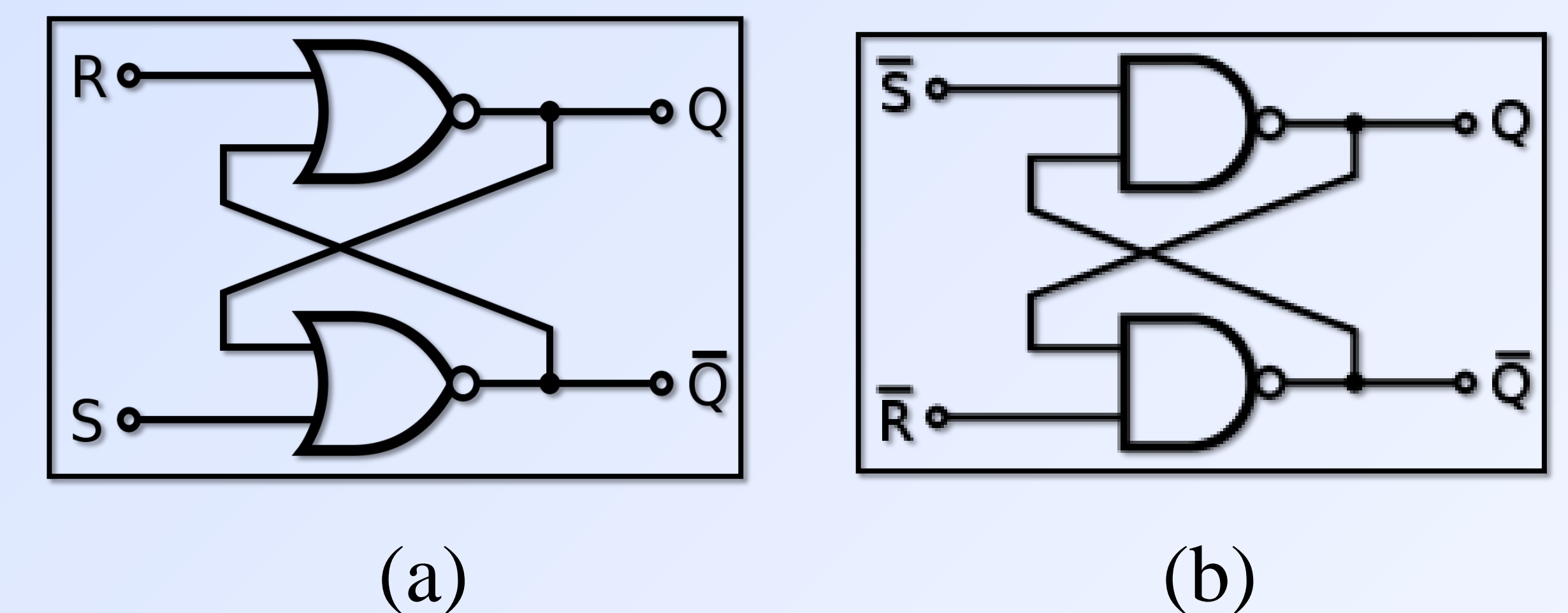


Figure 1. Core of (a) a NOR-gate SR flip-flop (b) a NAND-gate SR flip-flop

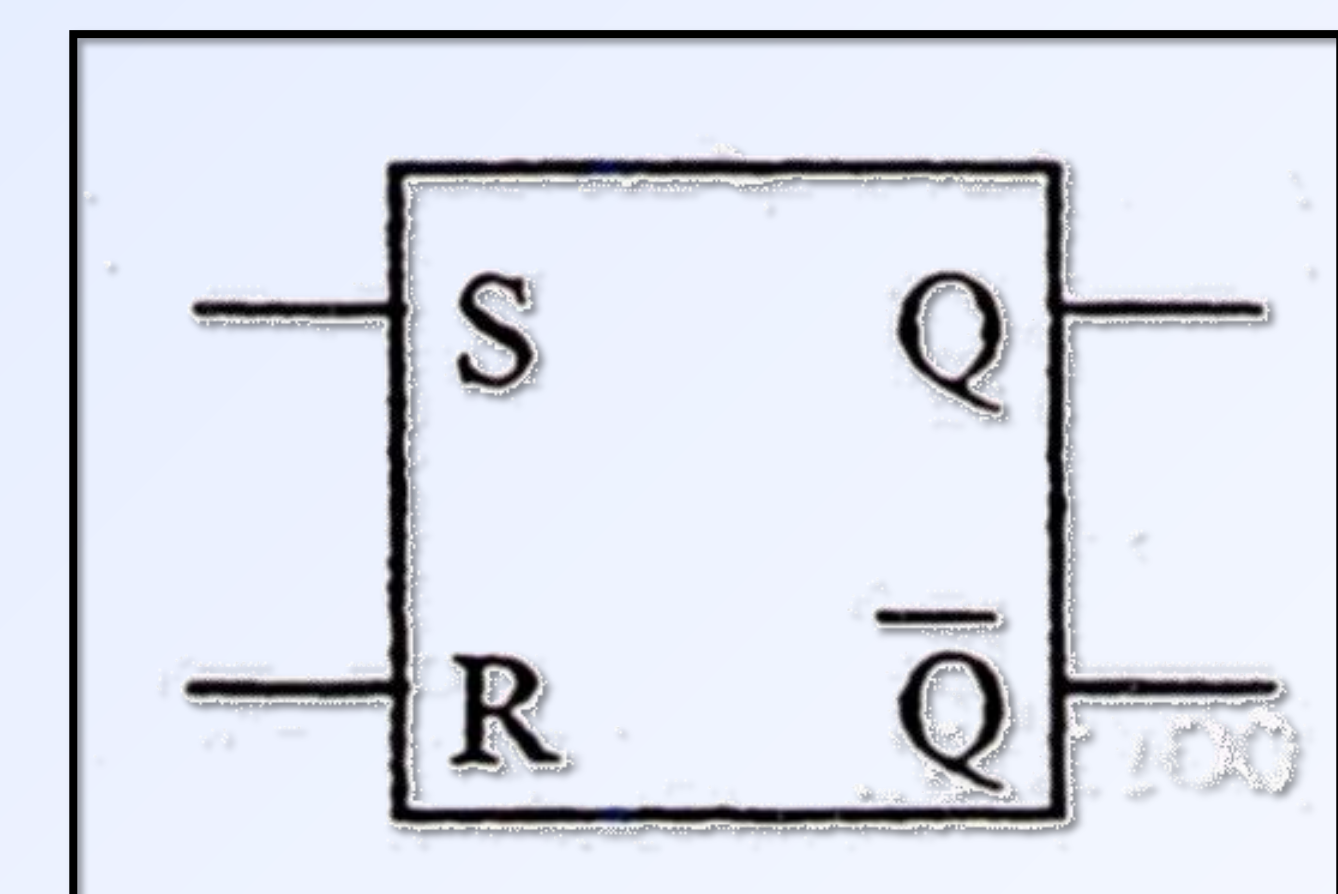
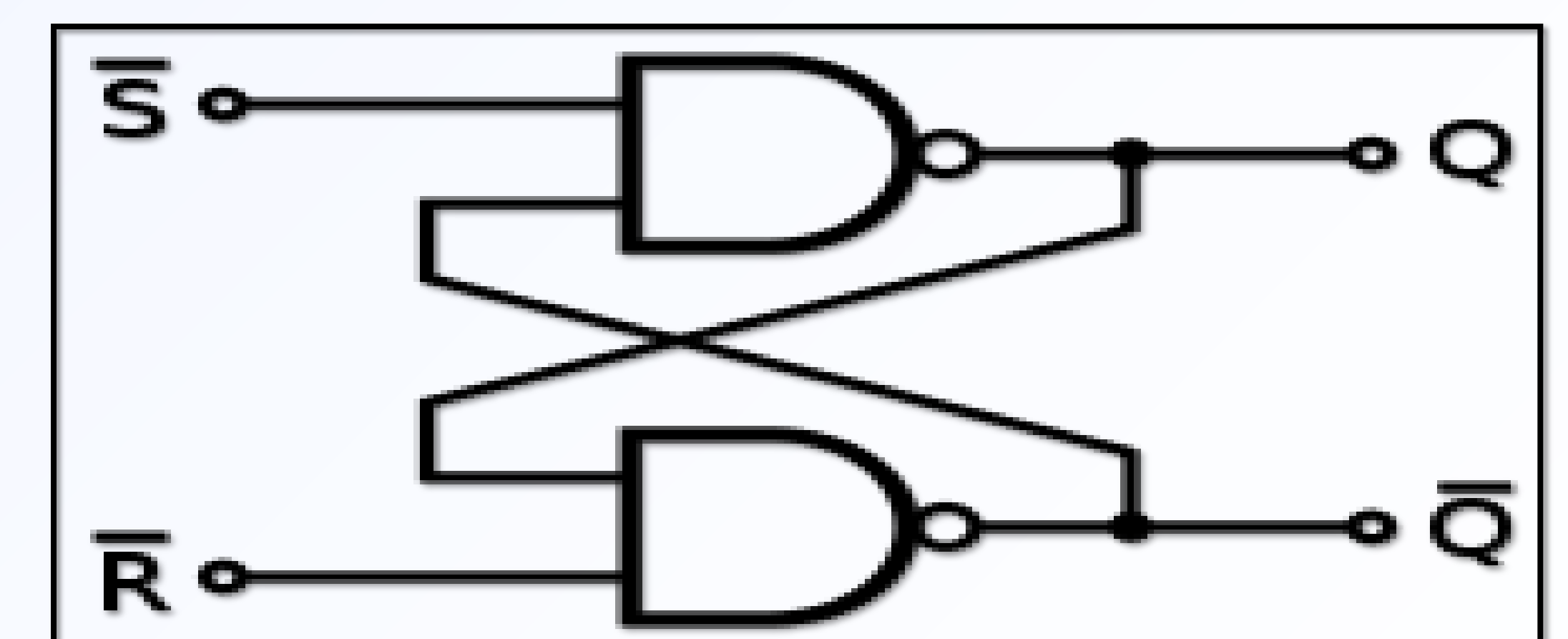


Figure 2. gate symbol of SR flip-flop

Procedures

First Experiments:

1. Connect the following circuit using 7400 NAND gate in the Prototyping board.
2. Connect two inputs to input switches.
3. Connect pin 1 (Q) to output LED.
4. Change switches 1 and 2 on and off and show the output of LEDS.
5. Record the results in the following table.

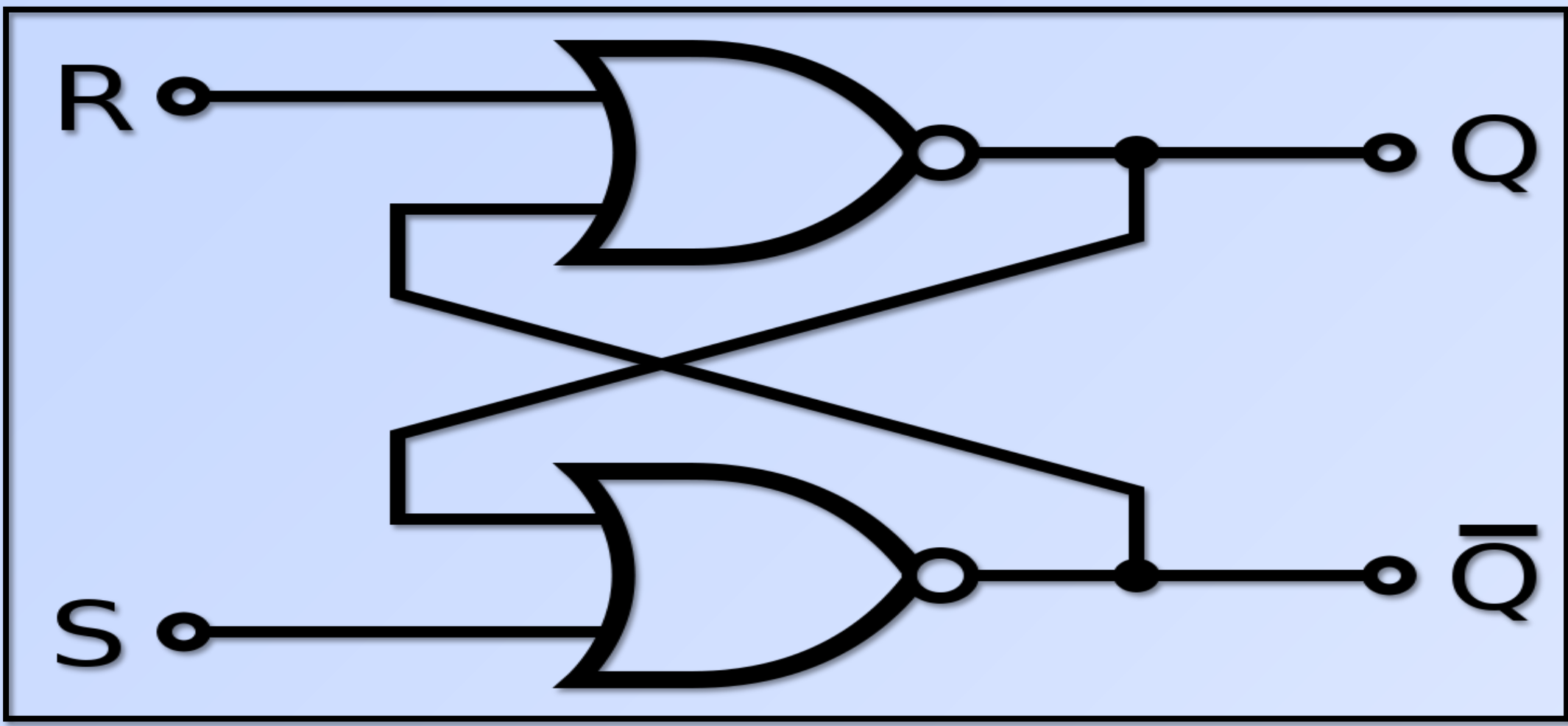


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Switch 1	Switch 2	Q^t	Q^{t+1}
S	R		
0	0		
0	1		
1	0		
1	1		

Second Experiments:

1. Connect the following circuit using 7402 NOR gate in the Prototyping board.
2. Connect two inputs to input switches.
3. Connect pin 1 (Q) to output LED.
4. Change switches 1 and 2 on and off and show the output of LEDS.
5. Record the results in the following table.



Switch 1	Switch 2	Q^t	Q^{t+1}
S	R		
0	0		
0	1		
1	0		
1	1		